Theoretical complexity of graph-analysis for electrical circuit error detection

Context

Aniah is a Start-up that offers tools for analyzing semiconductor manufacture circuits. Aniah has introduced algorithms relying on hierarchical graph decompositions that significantly pushes the boundaries of the size of analyzable circuits, from a few hundred thousand elements to several trillion. Aniah is collaborating with the Laboratoire de l'Informatique du Parallélisme (LIP) to consolidate and generalize its approach by supplementing its practical results with a theoretical backbone.

The start-up has proposed these hierarchical graph-analysis algorithms for detecting electrical errors. In this regard, the proposed algorithms operate by first discerning a number of well-known topologies in the designed circuit, then by using specific graph algorithms, the unexpected errors are detected. In general, most of the investigated problems by Aniah are NP-hard from a theoretical point of view [1, 2]. However, by modeling the investigated problems using graph theory, it becomes possible to solve practical instances properly using new graph algorithms [3, 4, 5].

Objectives of the internship

The objective of this internship is to conduct a deep theoretical study on the proposed graph-based approach. While the application domain is integrated circuits, we are looking for candidates interested in theoretical aspects, especially graph theory and complexity, for this internship. Prior knowledge of electronics notions is not mandatory. This study aims to investigate the time and space complexities of existing algorithms, improve current methods, and design new algorithms for specific graph optimization problems. The latter should be tested on practical cases. The trainee should be interested in the following research topics:

- topology detection: to detect a number of well-known electrical topologies by understanding the behavior of each electrical circuit in the corresponding graph model using graph optimization algorithms.
- graph decomposition: to use graph decomposition techniques for clustering the initial big instances then to analyze each sub instance (subgraph) independently by adopting new algorithms and thus reducing the time complexity.
- circuit simplification: to obtain an equivalent graph of a given circuit, one must detect templates and propose graph reduction rules that could simplify the initial graph and consequently design a simpler equivalent circuit.
- synthesizing the detected errors: after analyzing the hierarchical graph and detecting errors, the goal is to find the cause and the source of each error in the graph and output the detected cause variables.

The internship is a preliminary study. We expect the student to understand existing algorithm, propose new ones, and possibly experiment them with a prototype implementation. This internship could lead to a CIFRE thesis funding (i.e. a Ph.D. co-supervised by a laboratory and a company), where we would push the experimental aspects further.

Required profile

The candidate should be familiar with algorithm design, computational complexity, algorithmic graph theory, and graph decomposition, and at least one programming language. Basic knowledge of electronic circuits would be appreciated.

How to apply

Send an email to matthieu.moy@univ-lyon1.fr, remi.watrigant@univ-lyon1.fr and mehdi.khosravian@aniah.fr with your CV, a short text describing your motivation, and any document that can support your application.

Advisors

- Matthieu Moy, maître de conférences UCBL/LIP, `https://matthieu-moy.fr/`
- Remi Watrigant, maître de conférences UCBL/LIP, `http://perso.univ-lyon1.fr/remi.watrigant/`
- Mehdi Khosravian, Algorithm engineer in Aniah, `https://www.linkedin.com/in/mehdikhosravian/`

Place

- Laboratoire de l'Informatique du Parallélisme (LIP) – École Normale Supérieure de Lyon.
- Aniah, Grenoble.

References

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[2] Johannes Köbler, Uwe Schöning, and Jacobo Torán. *The Graph Isomorphism Problem: Its Structural Complexity*. Progress in Theoretical Computer Science. Birkhäuser/Springer, 1993.

[3] Maximilian Neuner and Helmut Graeb. Synergetic algorithm for power-down synthesis. In *2020 European Conference on Circuit Theory and Design (ECCTD)*, pages 1–5. IEEE, 2020.

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[5] Michael Zwerger and Helmut Graeb. Verification of the power-down mode of analog circuits by structural voltage propagation. *Analog Integrated Circuits and Signal Processing*, 78(1):177–189, 2014.