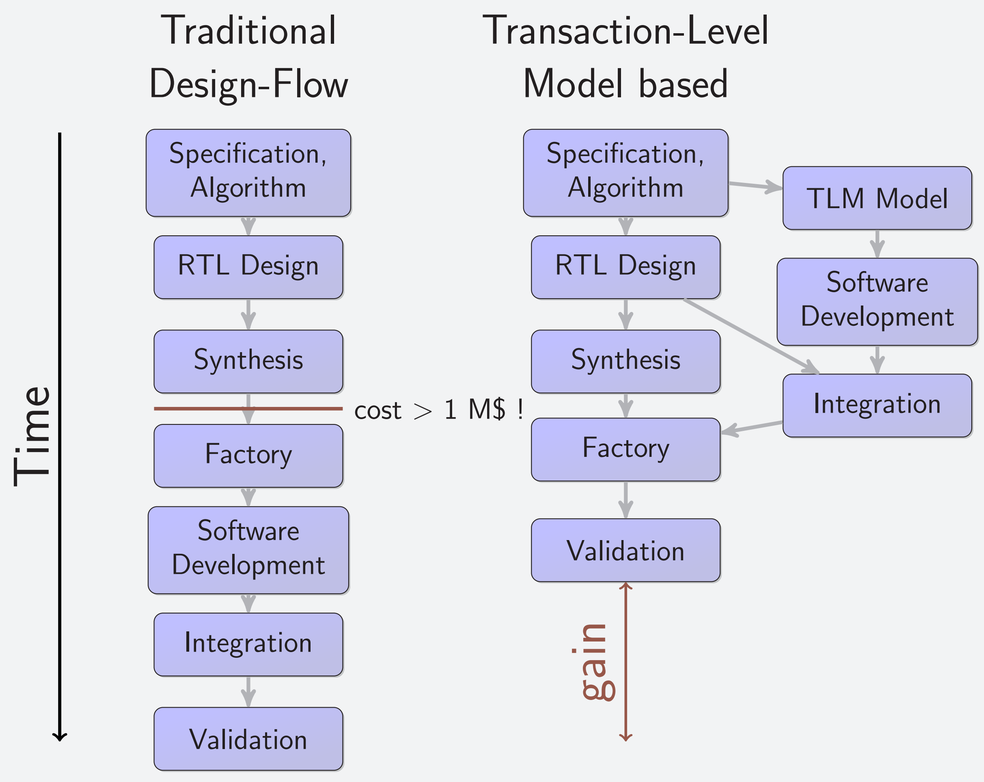
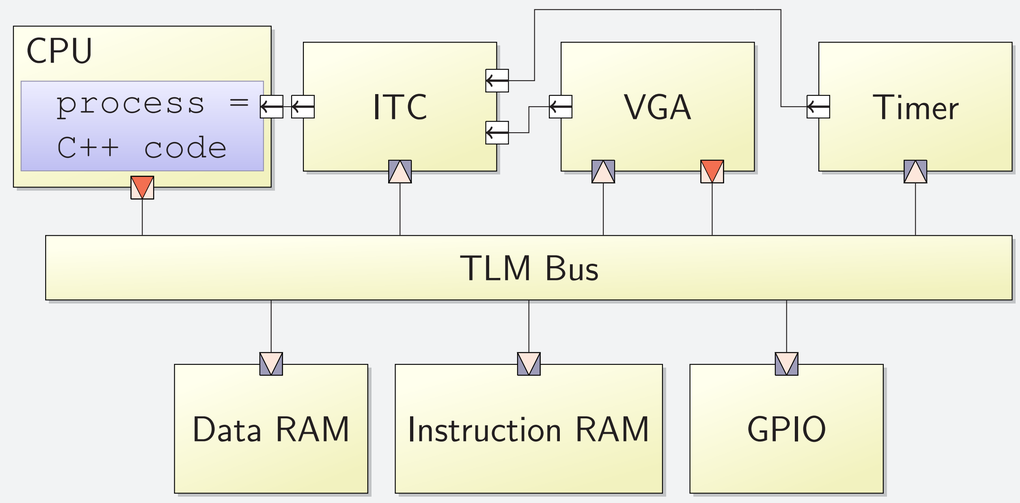
sc-during: Parallel Programming with SystemC for Loosely Timed Models

Matthieu Moy
Verimag / Grenoble INP

TLM design-flow



Example



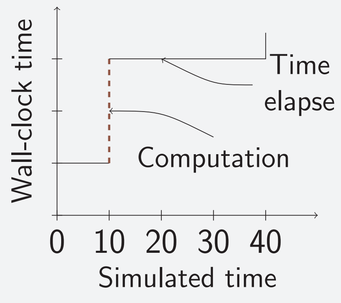
Uses of TLM

- Early software development
- Hardware verification
- Architecture exploration

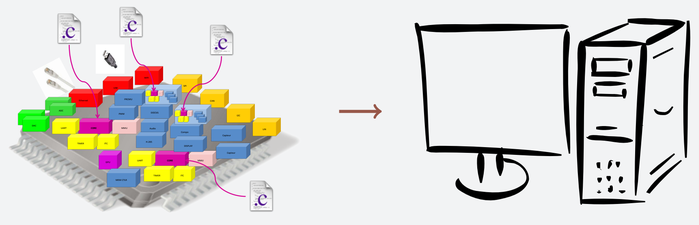
Contents of a model

- What is needed for software
- ... and only that

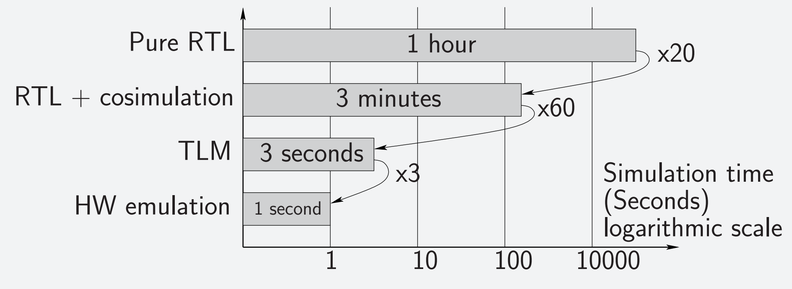
Simulated time



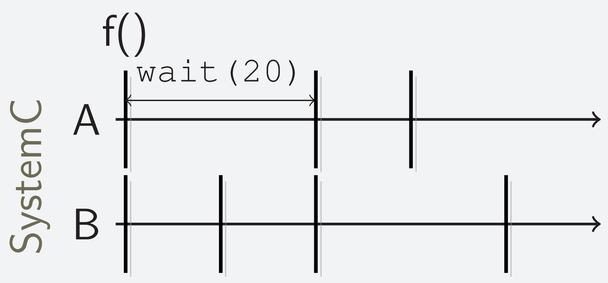
Simulation Parallelism



Simulation speed

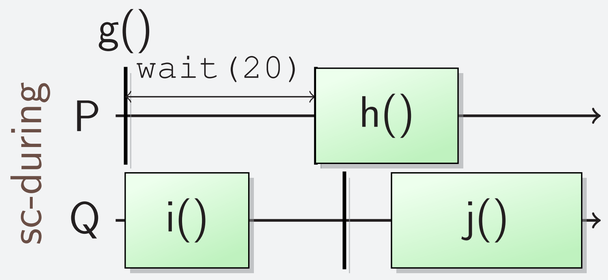


Tasks with Duration



Process A:

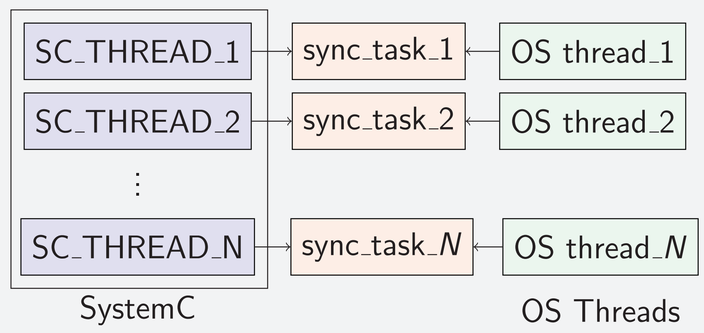
```
//Computation
f();
//Time taken by f
wait(20);
```



Process P:

```
g();
wait(20);
during(15, h);
```

Processes in SystemC and sc-during

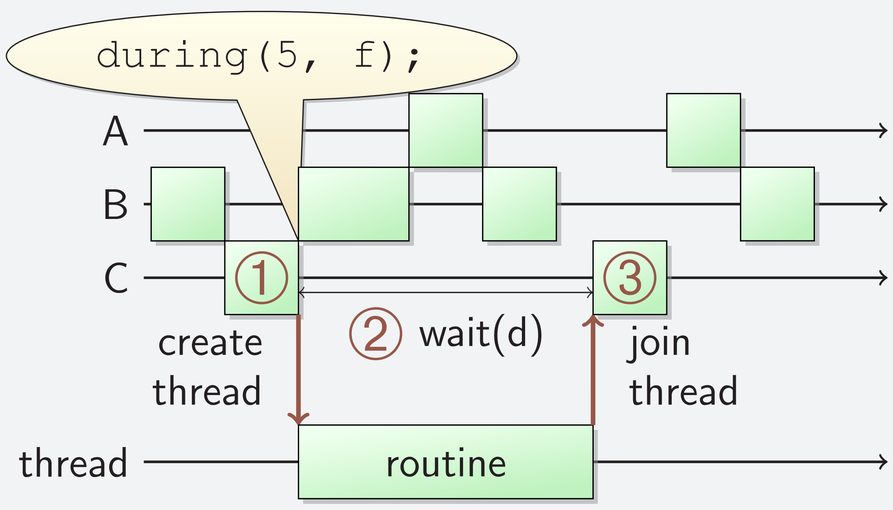


Possible strategies:

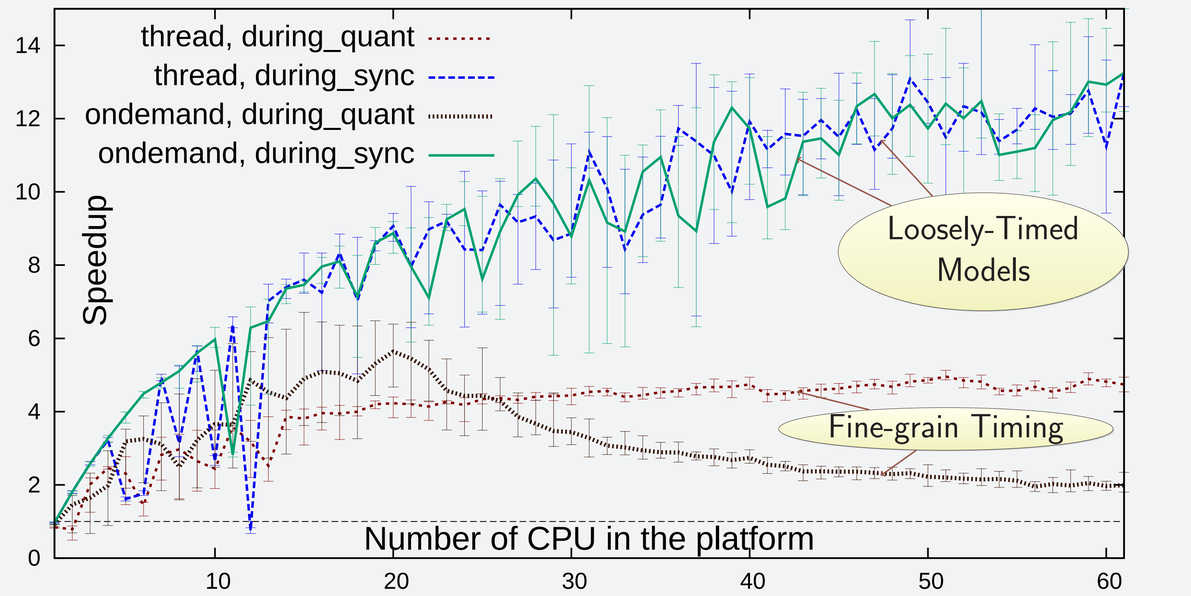
SEQ: Sequential (= reference)
THREAD: Thread created/destroyed each time
POOL: Pre-allocated worker threads pool
ONDEMAND: Thread created on demand and reused later

Sketch of implementation

```
void during(sc_core::sc_time duration,
            std::function<void()> routine) {
①   std::thread t(routine); // create thread
②   sc_core::wait(duration); // let SystemC execute
③   t.join(); // wait for thread completion
}
```



Results



Test machine has $4 \times 12 = 48$ cores

Try it!

- Open Source (< 1500 LOC)
- http://sc-during.forge.imag.fr/