Techniques et outils pour la vérification de systèmes-sur-puces au niveau transactionnel

Matthieu Moy

Synchronous Languages and Reactive Systems
Laboratoire Verimag, INPG

System Platform Group
STMicroelectronics

9 Décembre 2005

Jury:	Gérard Michel	Président
	Stephen Edwards	Rapporteur
	Jean-Pierre Talpin	Rapporteur
	Florence Maraninchi	Directrice
	Laurent Maillet-Contoz	Examinateur

Techniques and Tools for the Verification of Systems-on-a-Chip at the Transaction Level

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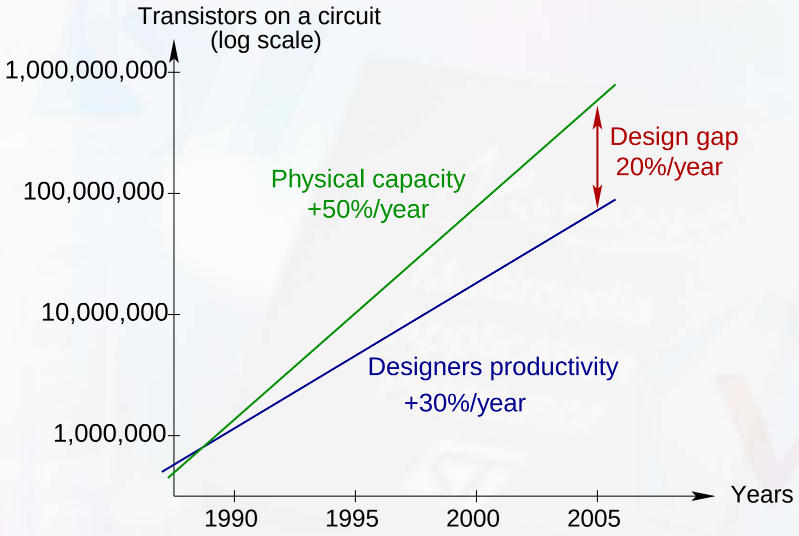
Objective of the Thesis

"Provide a connection from SystemC/TLM
to existing verification tools"

Outline

Outline

The Design Gap



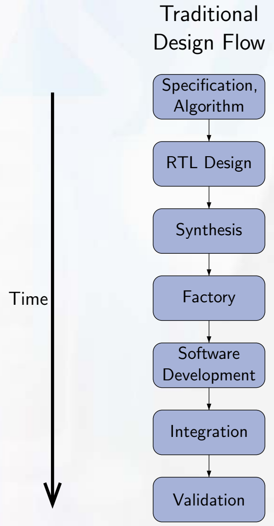
Hardware Vs Software

- Hardware
  - Fast
  - Power-efficient
- Software
  - Flexible
  - Reusable
  - Faster to write

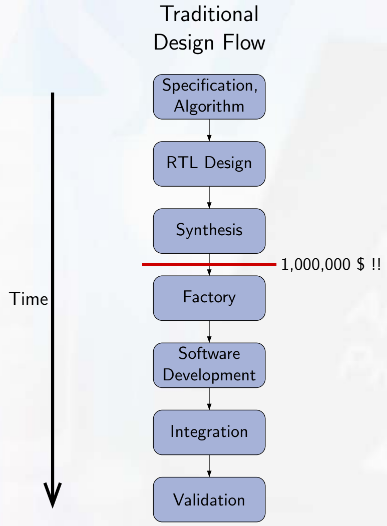
Hardware-Software Partitioning

- non-programmable ASIC: 100% Hardware
- General-purpose processors: 100% Software
- Systems-on-a-Chip (SoC): Mixture of Hardware and Software designed for each other

SoC Design Flow



SoC Design Flow



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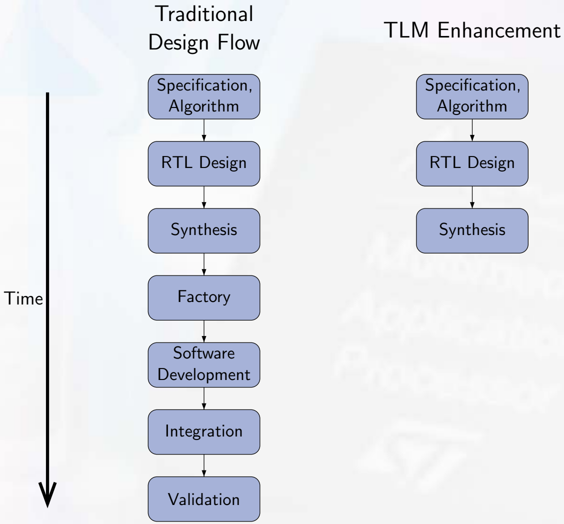

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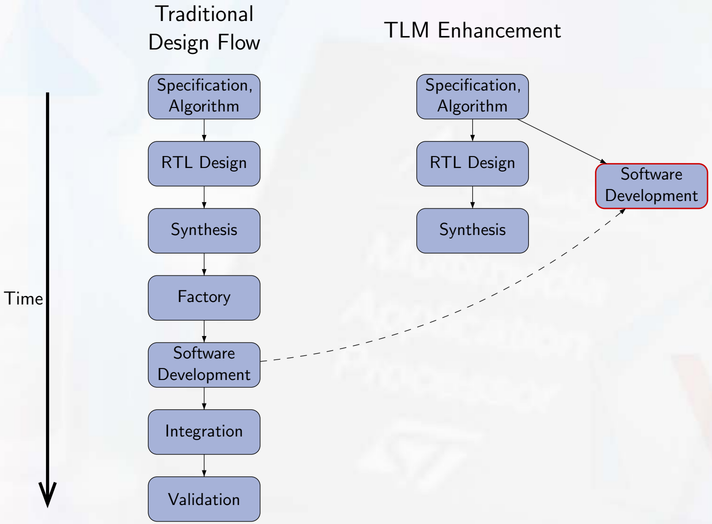

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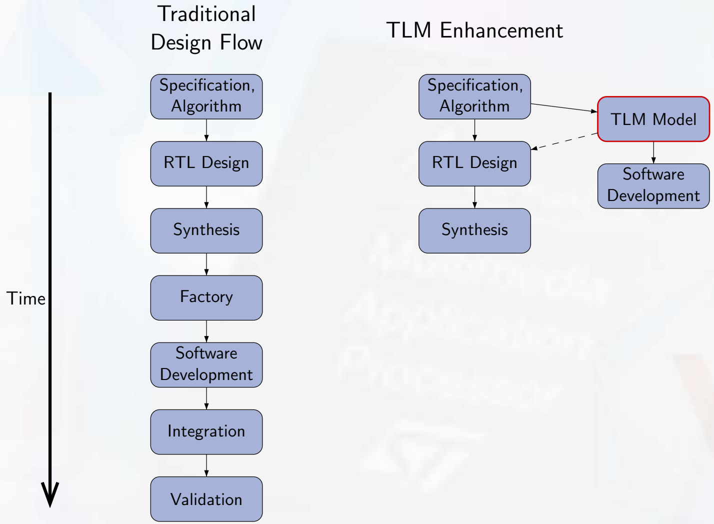

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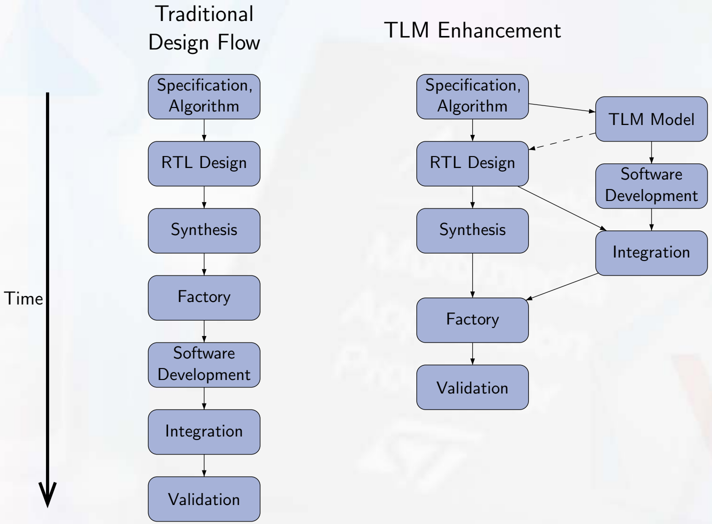

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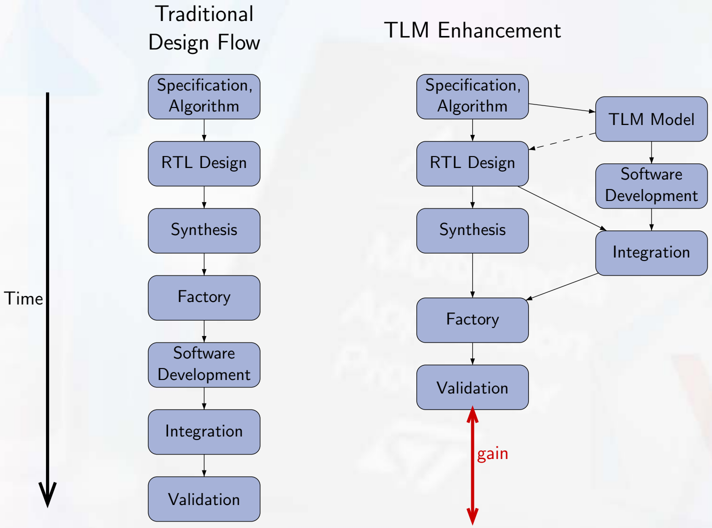


The Transaction Level Model: Principles and Objectives

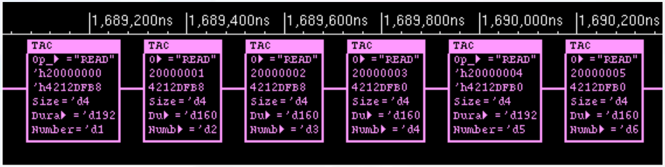
A high level of abstraction, that appear early in the design-flow

The Transaction Level Model: Principles and Objectives

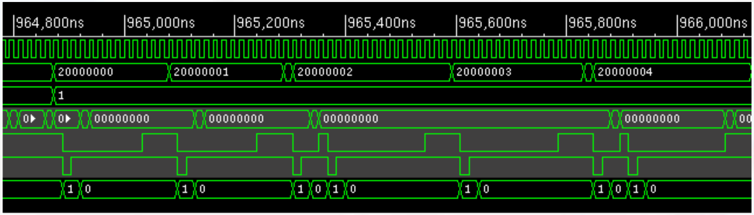
A high level of abstraction, that appear early in the design-flow

- A virtual prototype of the system, to enable
  - Early software development
  - Architecture exploration
  - Integration of components
- Abstract communication protocols and micro-architecture (remove implementation details from RTL)
  - Fast simulation ($\simeq$ 1000x faster than RTL)
  - Lightweight modeling effort ($\simeq$ 10x less than RTL)

The Transaction Level Model: Traces

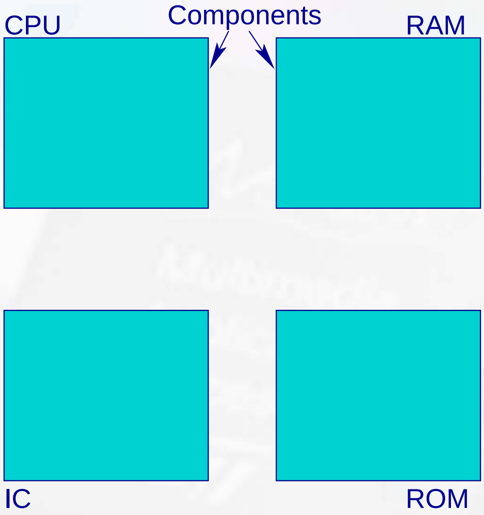

|1,689,200ns
|1,689,400ns
|1,689,600ns
|1,689,800ns
|1,690,000ns
|1,690,200ns
TAC op_▸ ="READ" 'h20000000 'h4212DFB8 Size='d4 Dura▸ ='d192 Number='d1
TAC o▸ ="READ" 20000001 4212DFB8 Size='d4 Du▸ ='d160 Numb▸ ='d2
TAC o▸ ="READ" 20000002 4212DFB8 Size='d4 Du▸ ='d160 Numb▸ ='d3
TAC o▸ ="READ" 20000003 4212DFB0 Size='d4 Du▸ ='d160 Numb▸ ='d4
TAC op_▸ ="READ" 'h20000004 'h4212DFB0 Size='d4 Dura▸ ='d192 Number='d5
TAC o▸ ="READ" 20000005 4212DFB0 Size='d4 Du▸ ='d160 Numb▸ ='d6

TLM: Transaction Level Model



RTL: Register Transfer Level

An Example TLM Model



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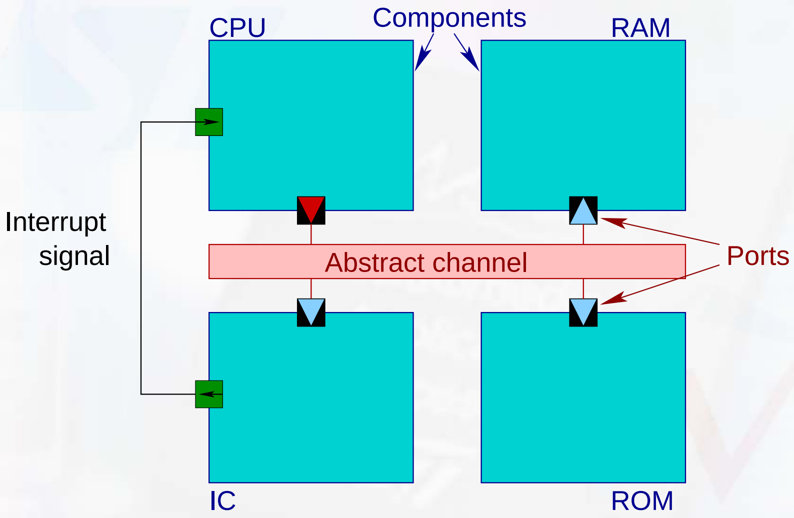

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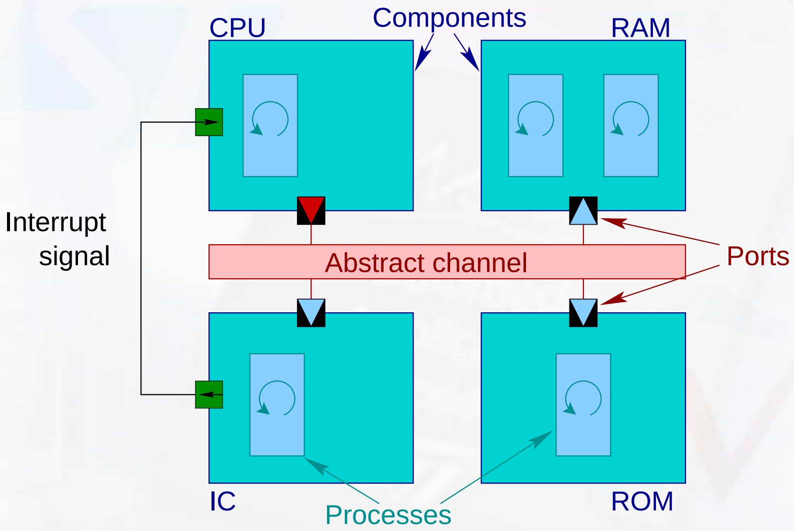
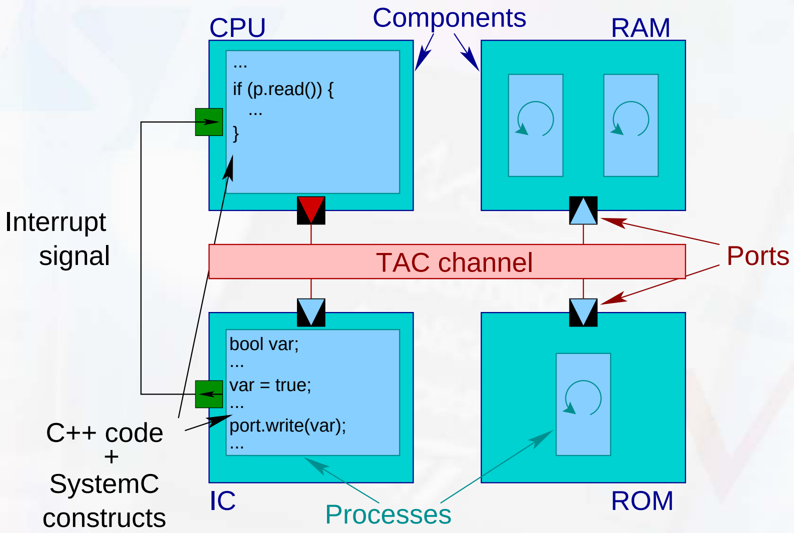


An Example TLM Model in SystemC



SystemC

- Useful to write Transaction Level Models

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- Library for C++ ($\Rightarrow$ compilable with any C++ compiler)
- Provides
  - Some objects usable directly (`sc_signal`, `sc_event`, ...)
  - Some base classes to be implemented (`sc_module`, ...)
  - An execution kernel (including a scheduler)

Why SystemC?

- For the industry:
  - Good support for TLM and heterogeneous systems
    - Simulates fast
    - Hardware/Software
    - TLM/RTL/Gate-level
  - Many available tools
    - from CAD vendors
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- As a research objective:
  - Used in the industry
  - Many case-studies available (no need to translate them)
  - Work on a portion of the real design-flow

Transaction Level Modeling in SystemC

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- SystemC provides the building blocks, but no high-level bus model
- Additional components are needed for TLM channels
- STMicroelectronics developed several bus models
  - BASIC: an example channel
  - TAC: a TLM channel used in production
- Will hopefully be standardized

Execution of a SystemC Program

- Architecture and Behavior
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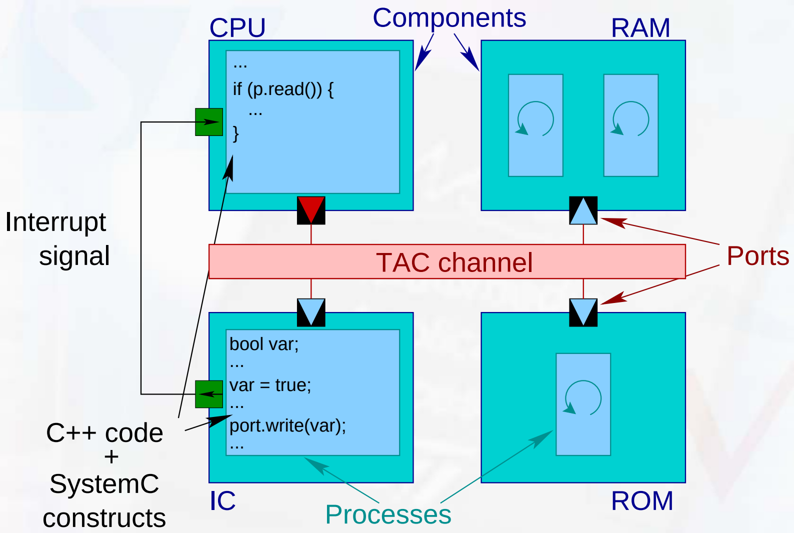
- Architecture and Behavior
  - No specific architecture description language
  - Arbitrary C++ can be used for both aspects
- Elaboration phase
  - Instantiate the components
  - Bind them together
- Simulation
  - Run the processes one by one
  - With a fixed architecture

An Example TLM Model in SystemC



Elaboration Phase: Build Architecture

```
int sc_main(int argc, char ** argv) {
   irq_controler  * ic = new irq_controler("IRQ");
   cpu * cpu = new cpu("CPU0");
   ram * ram = new ram("INT_RAM");
   rom * rom = new rom("ROM");
   tac_channel * channel = new tac_channel("CHANNEL");
   sc_signal<bool> sig;
   cpu->master_port.bind(channel->slave_port);
   ic->slave_port.bind(channel->master_port);
   ram->slave_port.bind(channel->master_port);
   rom->slave_port.bind(channel->master_port);
   ic->port.bind(sig);
   cpu->p.bind(sig);
   sc_start();
}
```

Elaboration Phase: Build Architecture

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// Main function
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// Components Instantiation (creation of C++ objects)
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// Binding (link between objects)
   cpu->master_port.bind(channel->slave_port);
   ic->slave_port.bind(channel->master_port);
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   ram->slave_port.bind(channel->master_port);
   rom->slave_port.bind(channel->master_port);
   ic->port.bind(sig);
   cpu->p.bind(sig);
// Start simulation (let the kernel execute processes)
   sc_start();
}
```

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Importance of TLM in the design flow

- No automatic synthesis from TLM to RTL
- A complement for RTL (not a replacement)

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- Embedded software is developed and tested partly on the TLM model

$\Rightarrow$ Although TLM models are not embedded in the chip, their validation is important

State of the Art

- Semantics of SystemC
  - Several papers for a semantics of RTL SystemC (very strict subset)
  - Usually do not take into account the real semantics of the scheduler
- Verification of TLM models
  - Recent research area
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  - Recent research area
  - Almost nothing relevant when we started
- In the meantime ...
  - Several tools for SystemC (front-ends, verification, lint, . . .)
  - Published work usually target a lower abstraction level than TLM as we use it in STMicroelectronics

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- Main choices
  - Deal with real SystemC code
  - Fully automated tool-chain
  - As few abstractions as possible
- Consequences
  - We need a front-end to read the SystemC code
  - We need a semantics for SystemC
    $\Rightarrow$ Formal, Simple, Executable

Expressing properties

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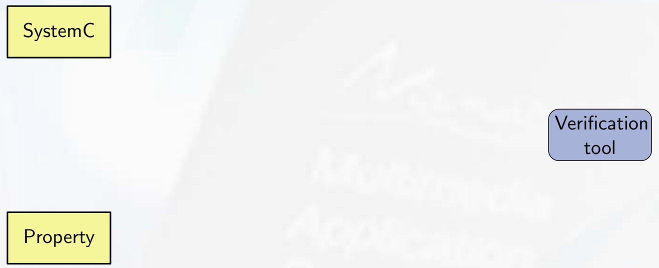
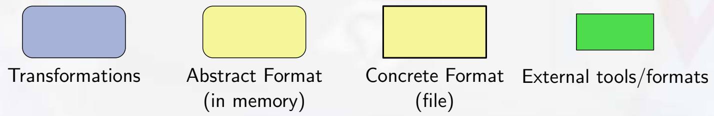
- No new specific language
- Express properties in C++/SystemC
  - `ASSERT(x.read() == true)`
- Use generic properties (things that you *usually* don't want)
  - Global dead-lock
  - Multiple write on a `sc_signal`
  - Process termination
  - Mutual exclusion

The LUSSY Tool Chain





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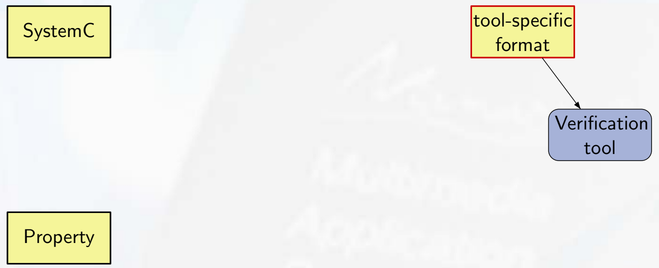

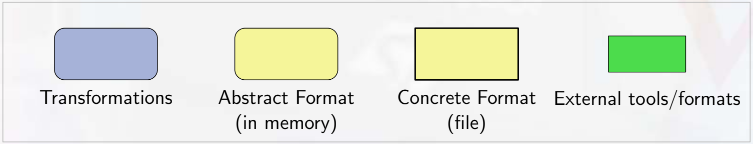

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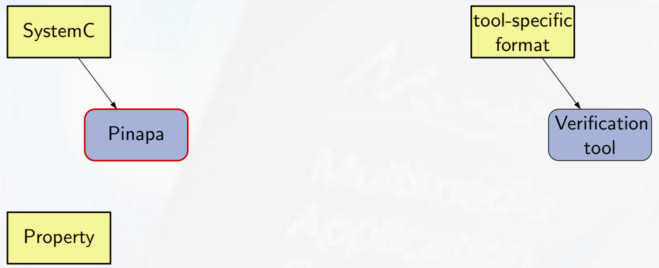

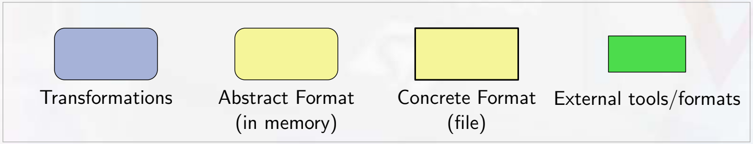

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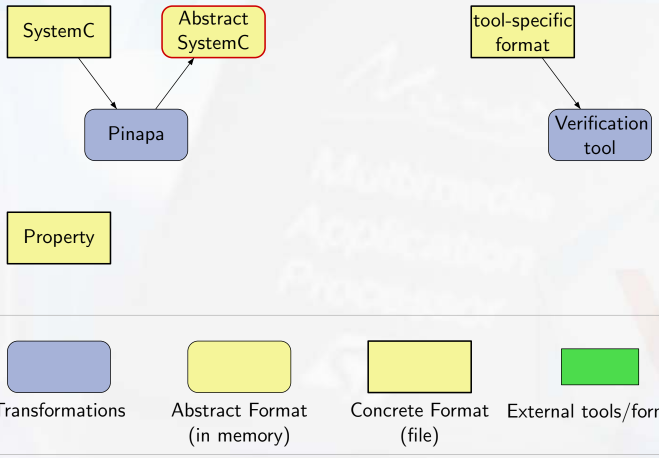

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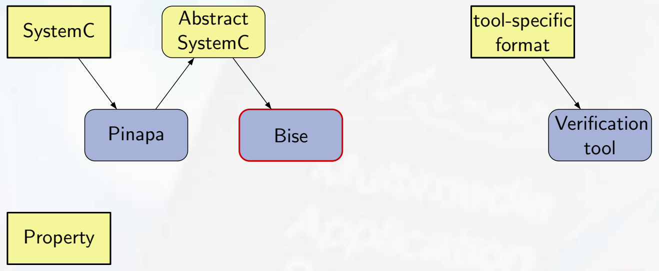

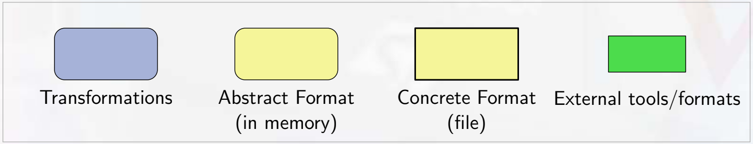

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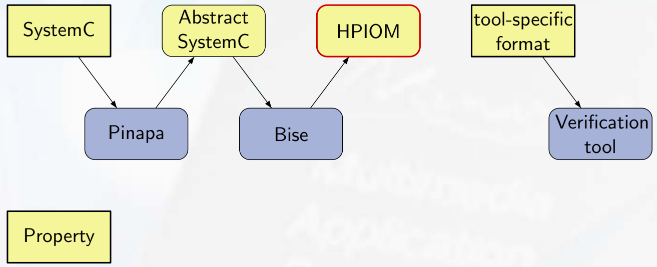

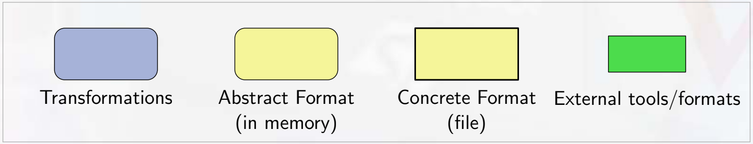

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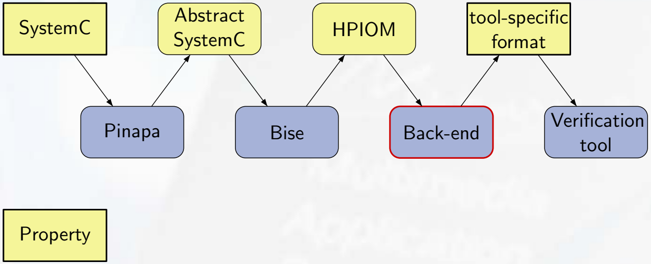

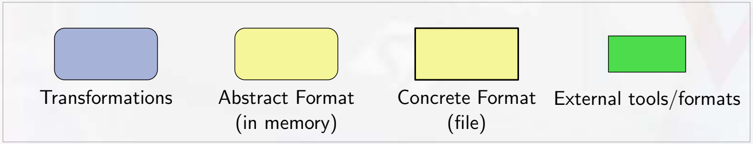

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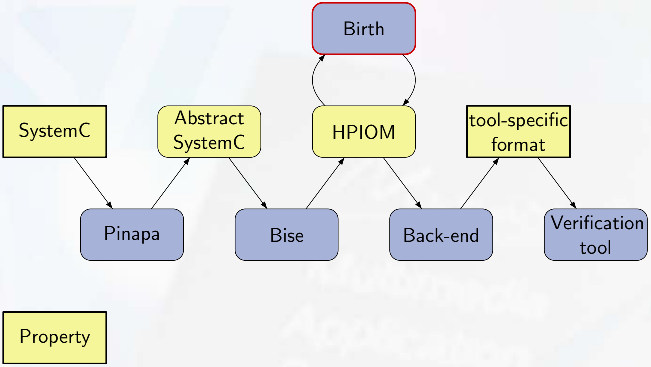

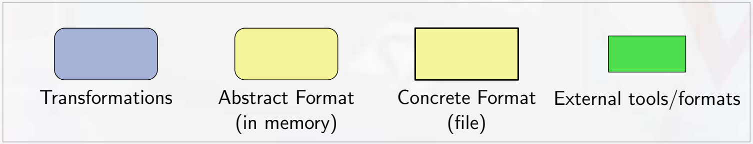

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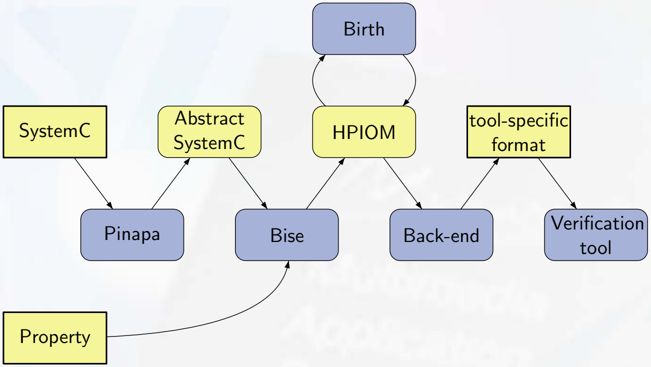

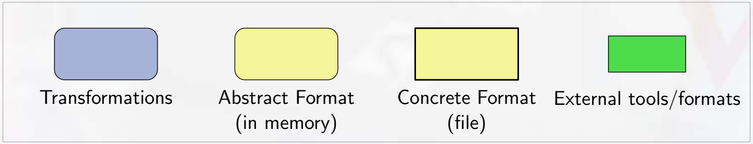

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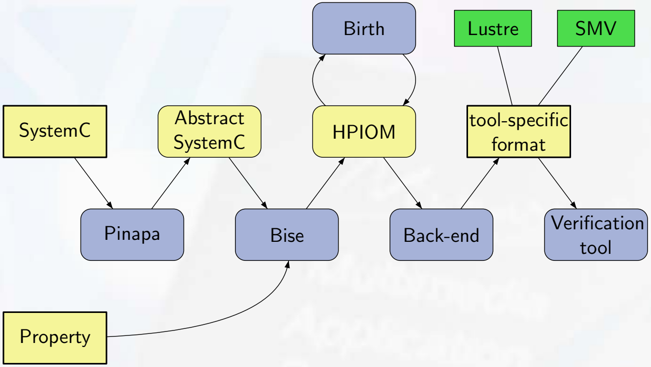

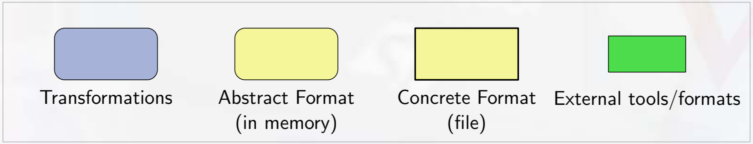

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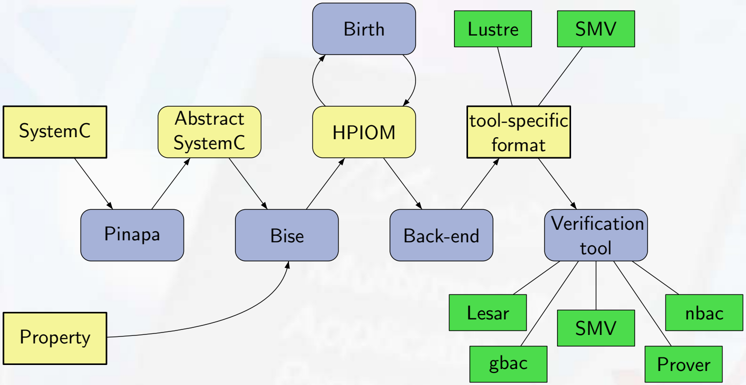

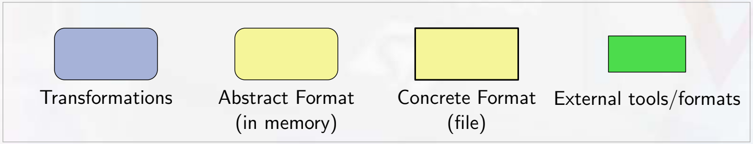

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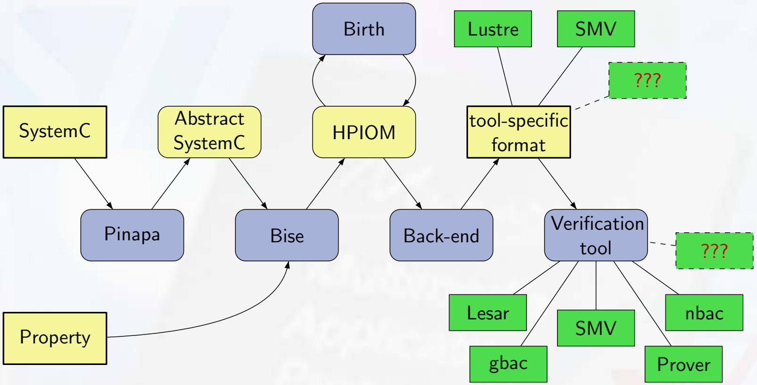

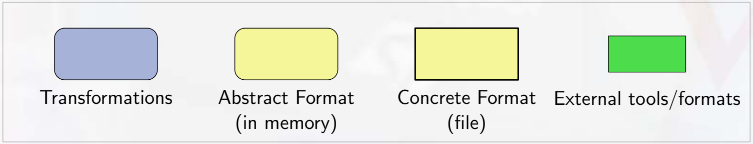

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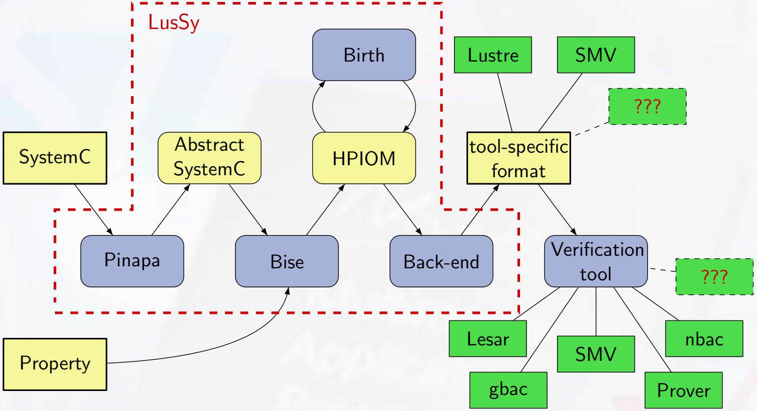
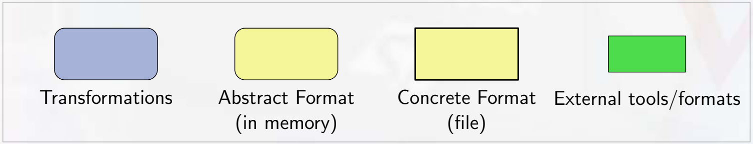
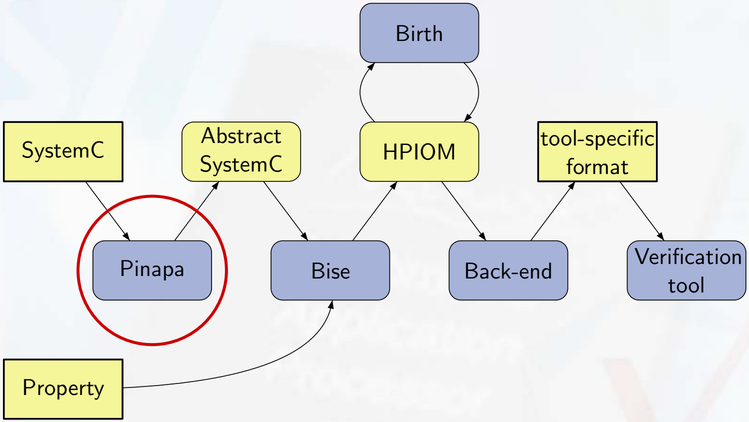




Outline

PINAPA: Pinapa Is Not A PArser



Main Choices

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- Use a C++ front-end, and nothing else
  $\Rightarrow$ Misses important information like architecture, built at run-time
- Use a C++ front-end, and recognize patterns in the elaboration phase
  $\Rightarrow$ Big limitation on the coding style of the elaboration

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- Write a grammar from scratch
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- Use a C++ front-end, and recognize patterns in the elaboration phase
  ⇒ Big limitation on the coding style of the elaboration
- Use a C++ front-end, and execute the elaboration phase to get the architecture
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Main Choices

There are many ways to “parse” SystemC:

- Write a grammar from scratch
  $\Rightarrow$ Needs to take all the C++ grammar into account!
  ParSyC, SystemPerl, sc2v, KaSCPar
- Use a C++ front-end, and nothing else
  $\Rightarrow$ Misses important information like architecture, built at run-time
- Use a C++ front-end, and recognize patterns in the elaboration phase
  $\Rightarrow$ Big limitation on the coding style of the elaboration
  SystemCXML, CoCentric
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  Approach chosen for PINAPA

Static Vs Dynamic Information in SystemC Programs

Information in SystemC	C++ compiler	Pinapa
Static		
Dynamic		

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Static: Lexicography, Syntax		
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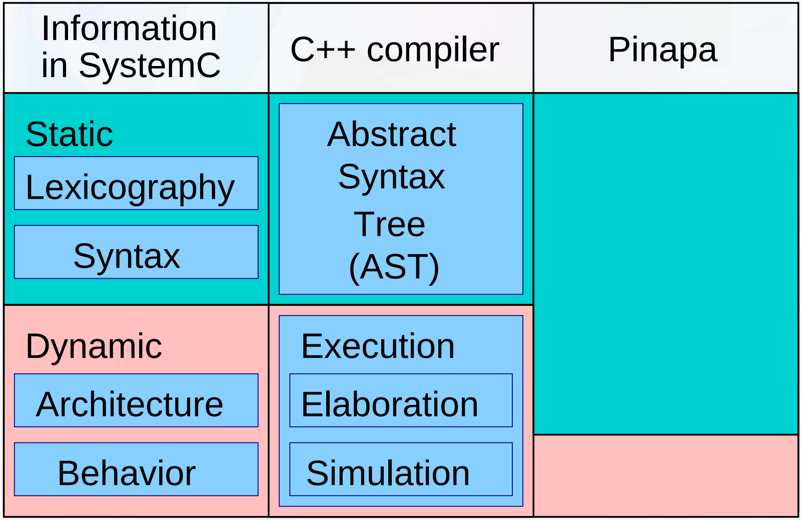
Static Lexicography Syntax	Abstract Syntax Tree (AST)	
Dynamic Architecture Behavior	Execution Elaboration Simulation	

Static Vs Dynamic Information in SystemC Programs



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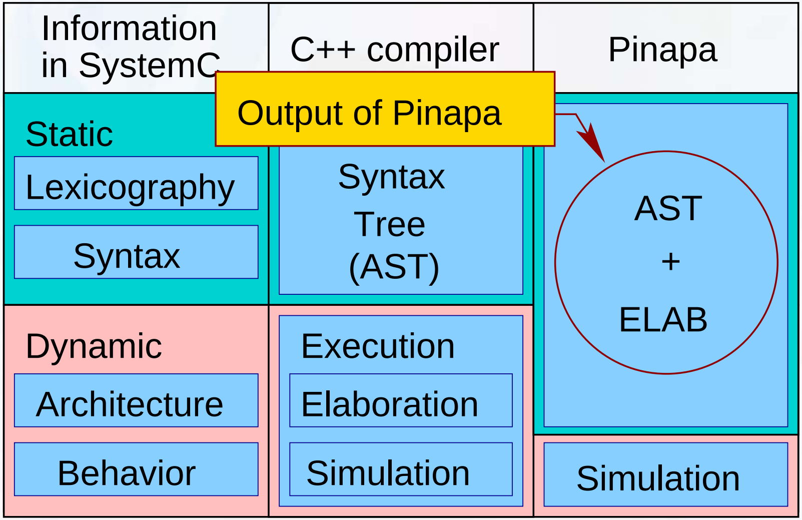

PINAPA: Key Ideas

- Syntax extraction (AST)
  - Easy if you have a C++ parser
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Then, what's difficult??

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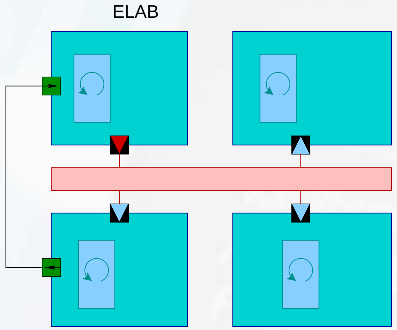
- We have to link the syntax and architecture information

Link Between ELAB and AST



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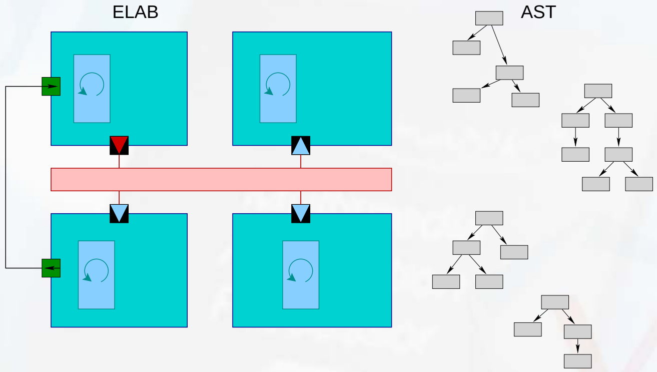

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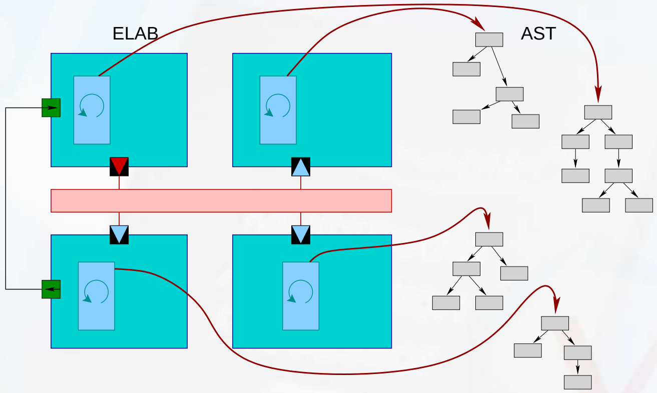

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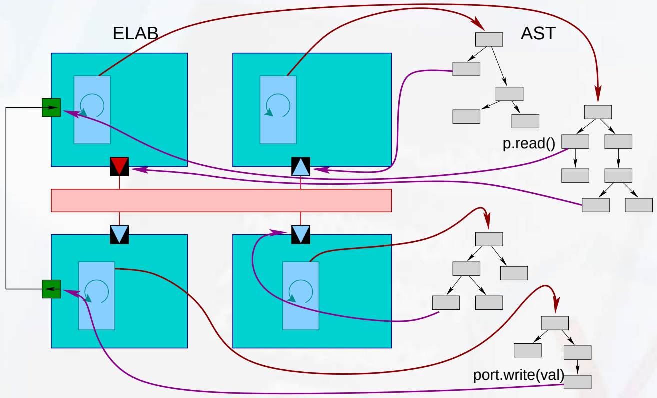

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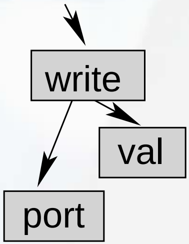

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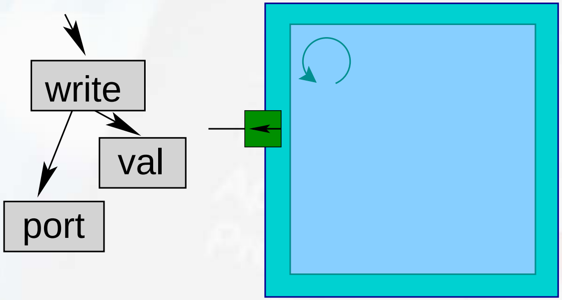

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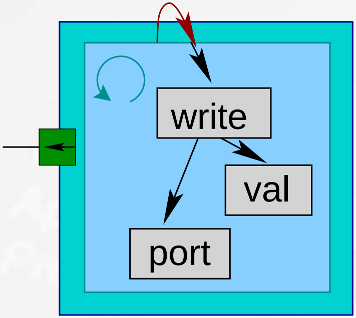

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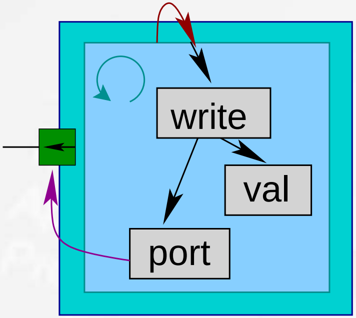

PINAPA: steps of execution

SystemC program

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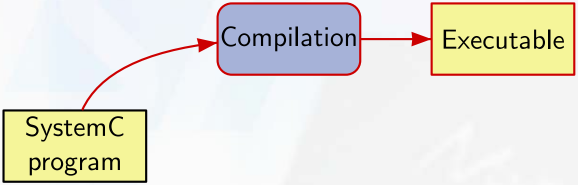

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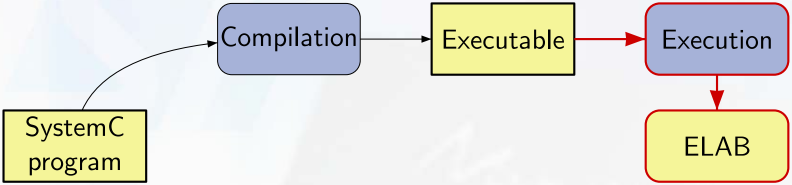

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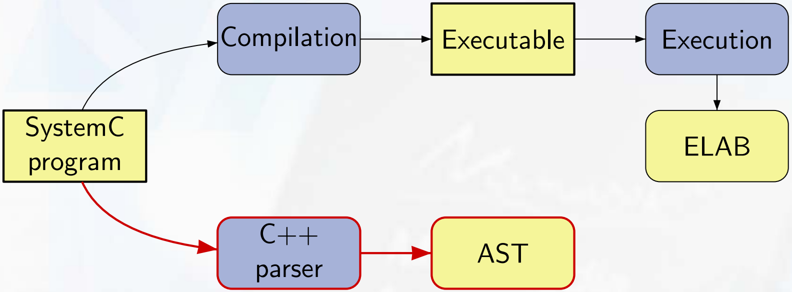

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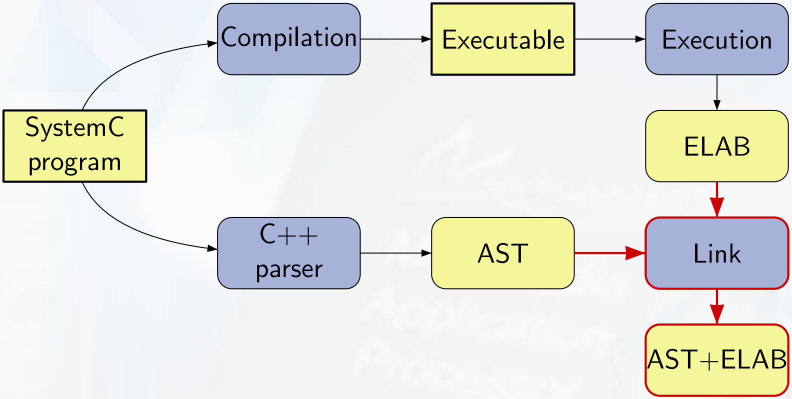

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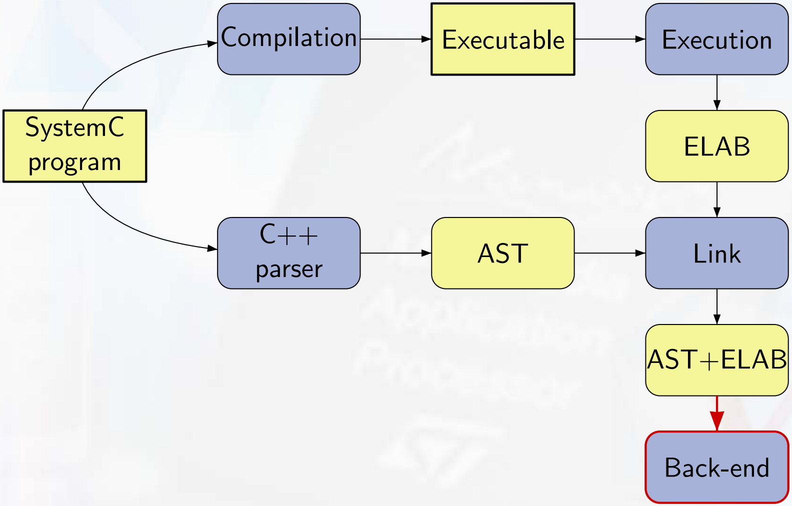

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Conclusion about PINAPA

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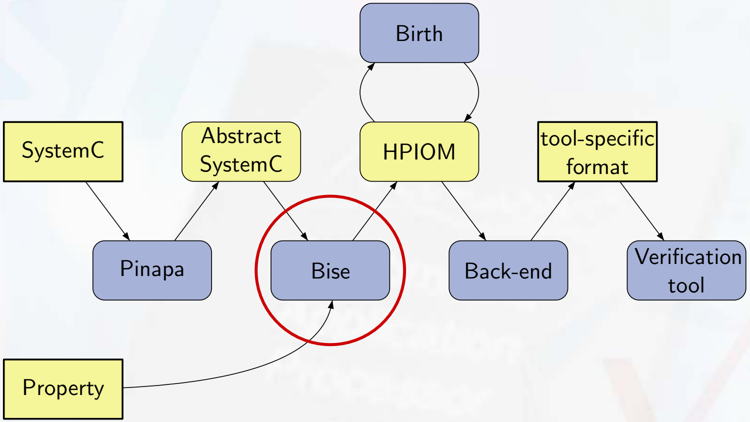
- PINAPA is Open Source!
  $\Rightarrow$ `http://greensocs.sourceforge.net/pinapa/`

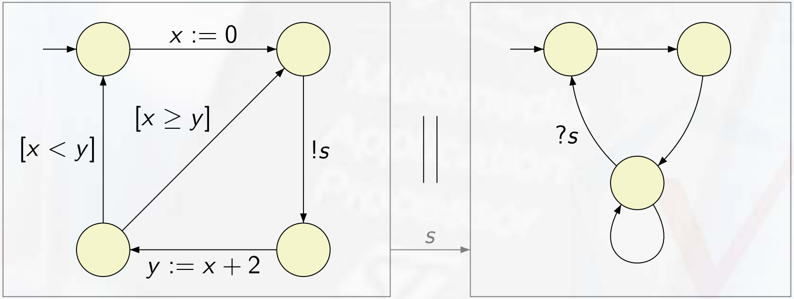
Outline

BISE: Back-end Independent Semantics Extraction



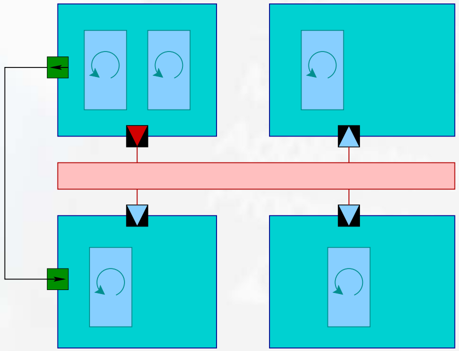
HPIOM: Heterogeneous Parallel Input/Output Machines

- A formalism of communicating automata
- With both explicit states and variables
- Using a synchronous product



Semantics of SystemC in terms of automata

- Generate a set of automata including:



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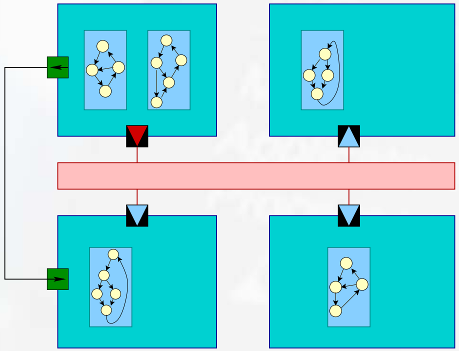

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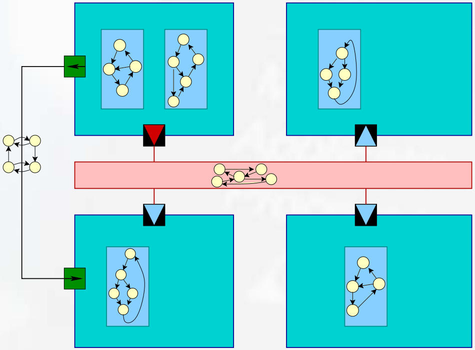

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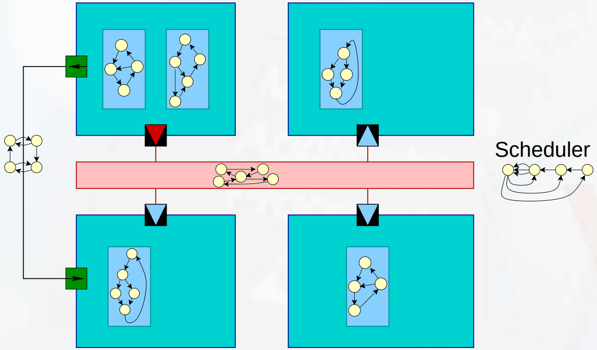

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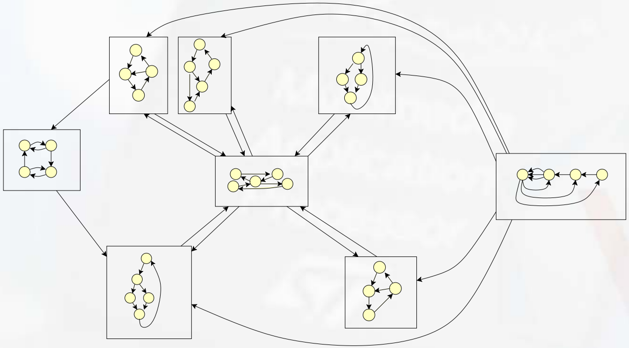

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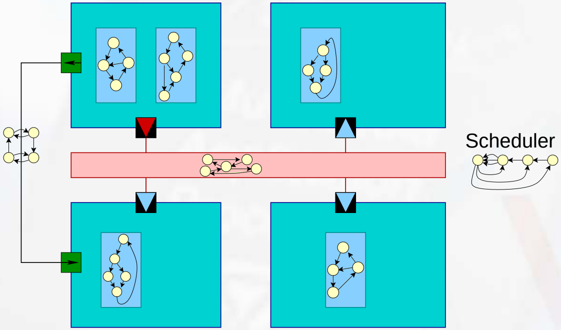

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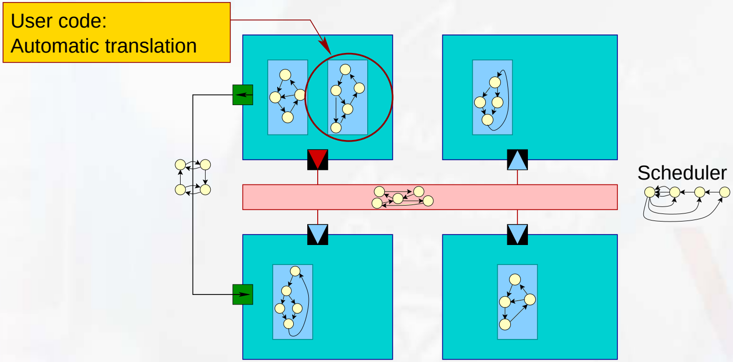

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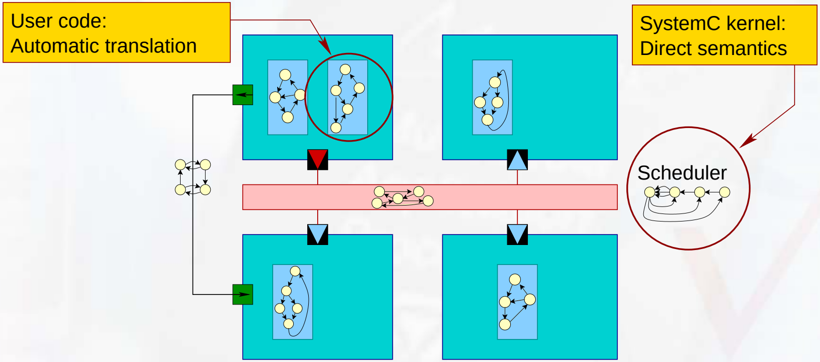

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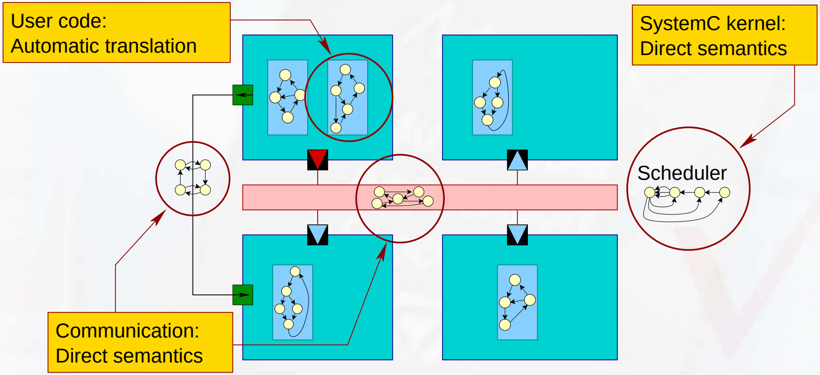
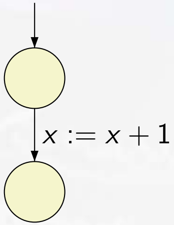


Translating C++ code into HPIOM

- Nothing new, but has to be done . . .

```
x = x + 1;
```



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x = x + 1;
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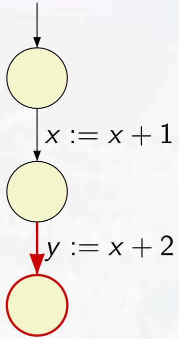

Translating C++ code into HPIOM

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```
while (x <= 3) {
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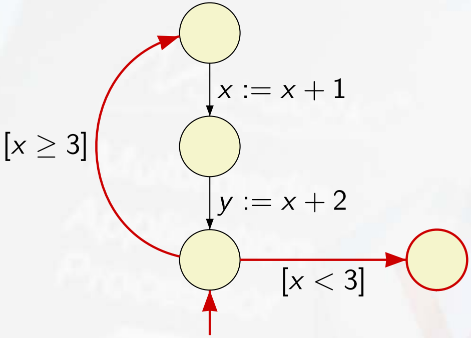
}
```



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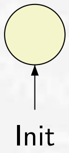

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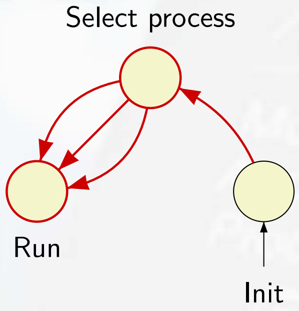

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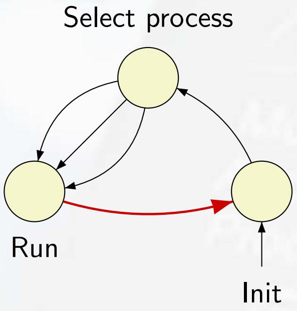

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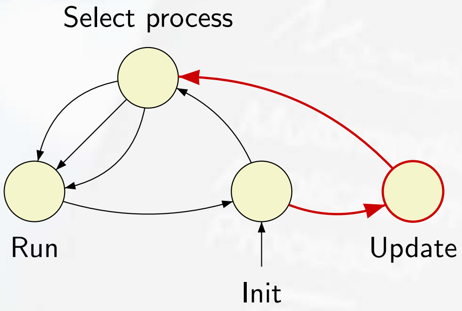

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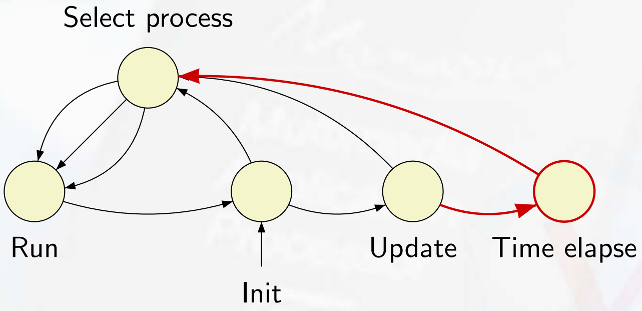

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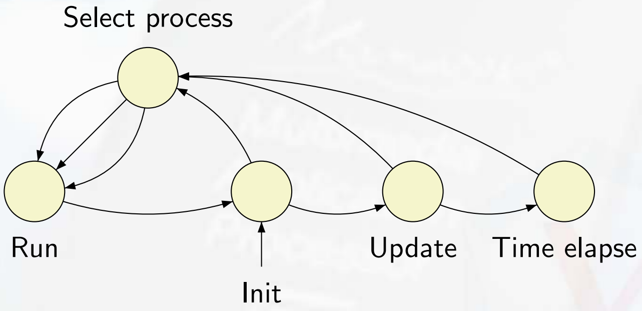

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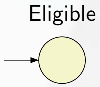

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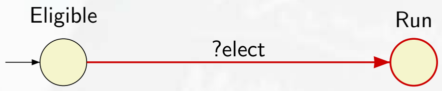

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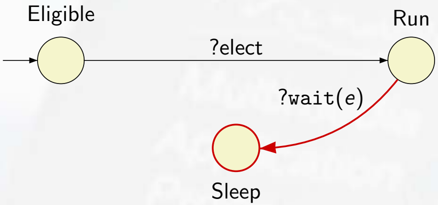

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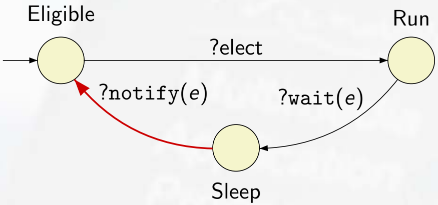

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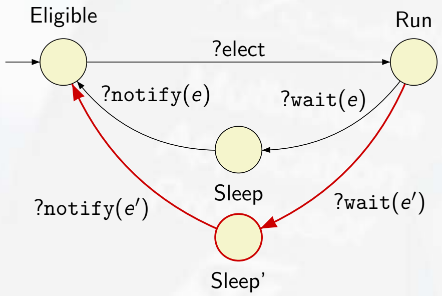

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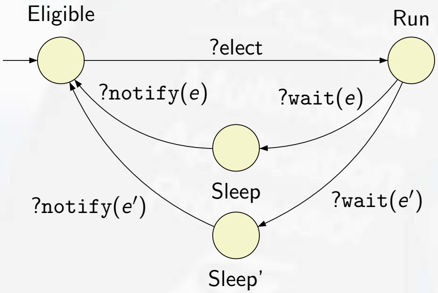

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Current value	
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		Current value	
		True	False
Next value	True		
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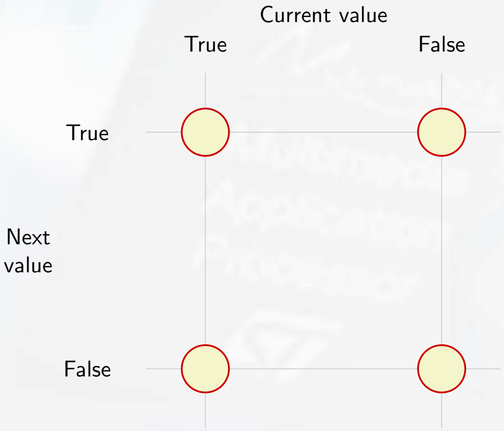

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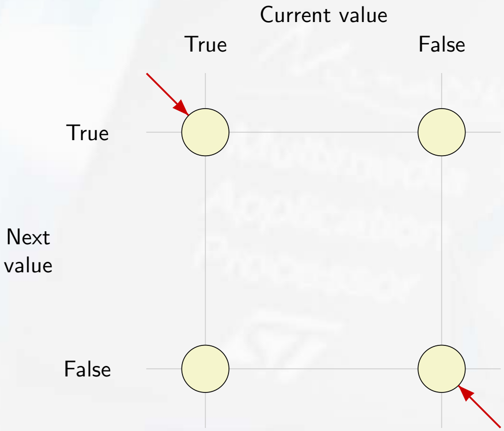

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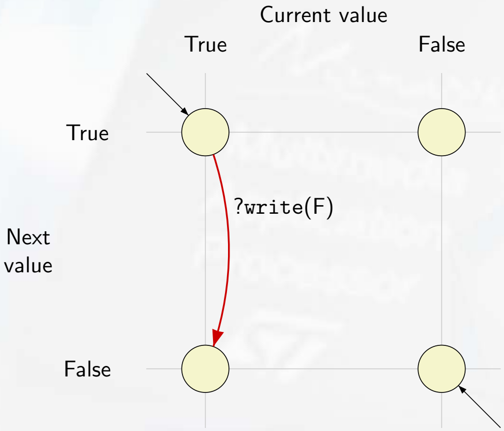

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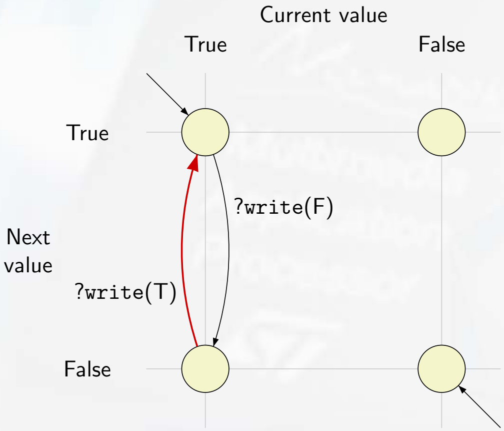

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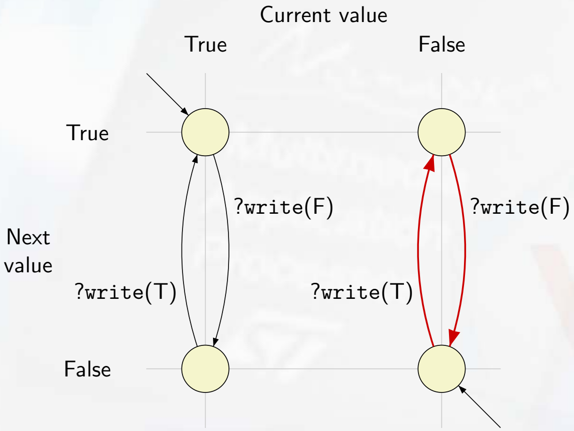

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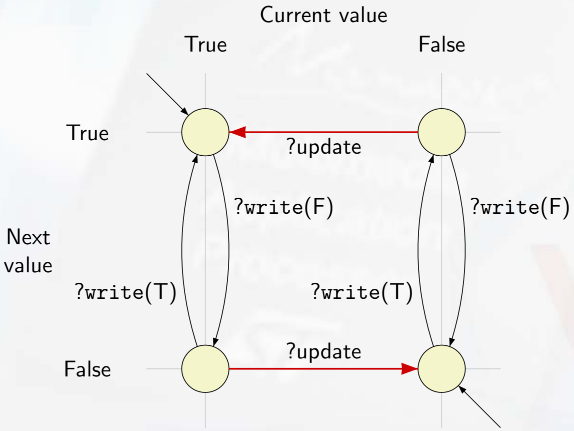

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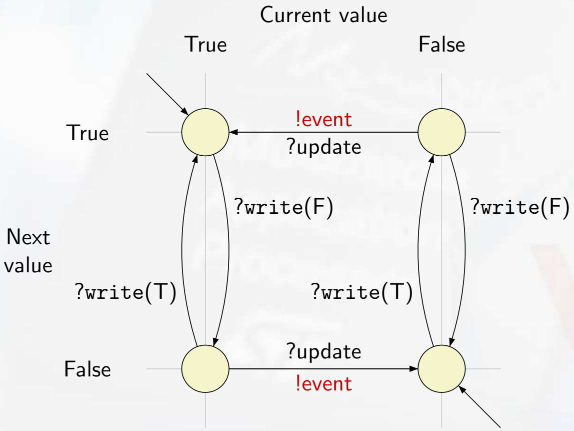

Semantics of SystemC Boolean Signals

- SystemC `sc_signal` avoids scheduling dependencies:
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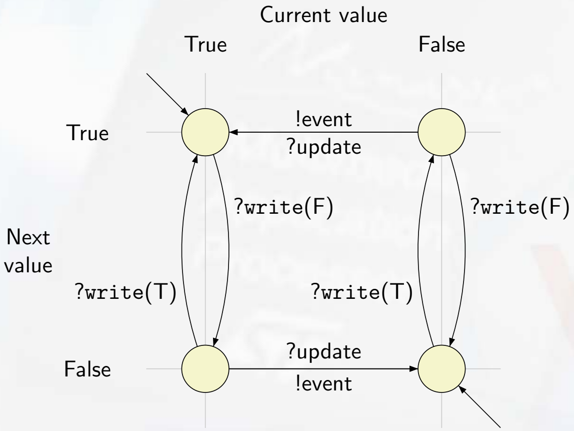
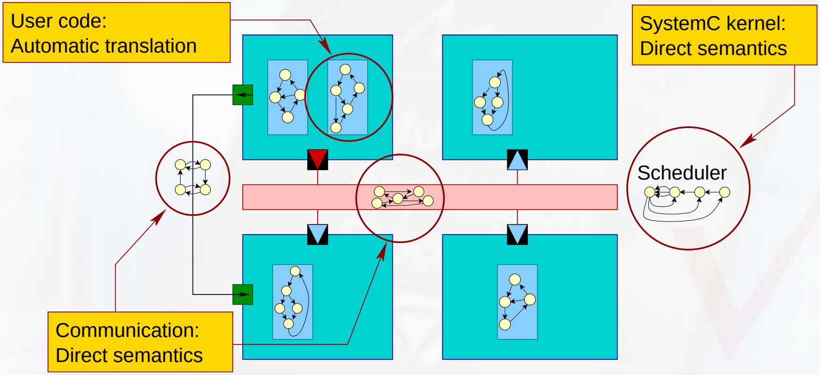


Direct Semantics Vs Translation

- Translation = Parse the source code, generate an automaton
- Direct semantics = Read the specification, instantiate an automaton



Outline

Other components not detailed here

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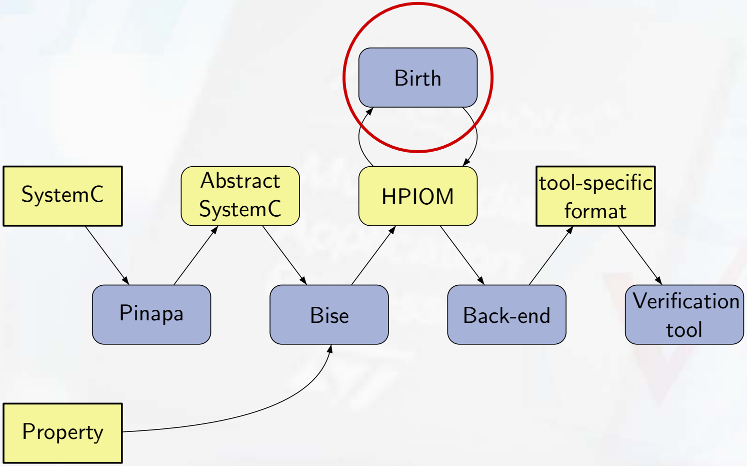

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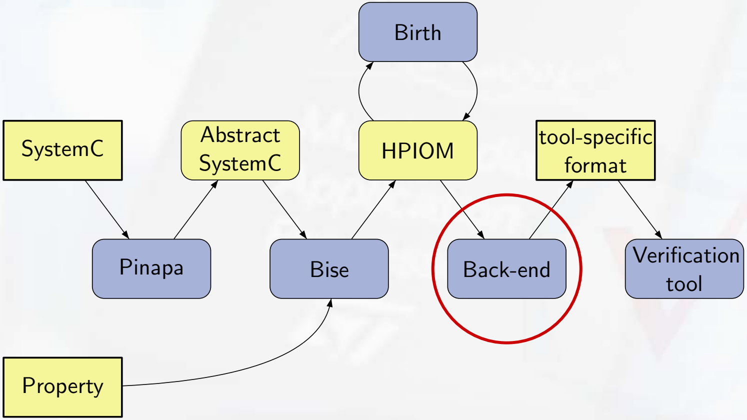

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So, is this work useless in practice?

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- Accurate modeling of SystemC semantics
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  - But state explosion on medium and large programs
- LUSSY provides the building blocks, but a lot is still to be done . . .

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  - Extensive use of abstract interpretation

    ⇒ Mathias Peron, Ph.D at Verimag

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    $\Rightarrow$ Experiments with PROMETHEUS (Yvan Roux, INRIA)
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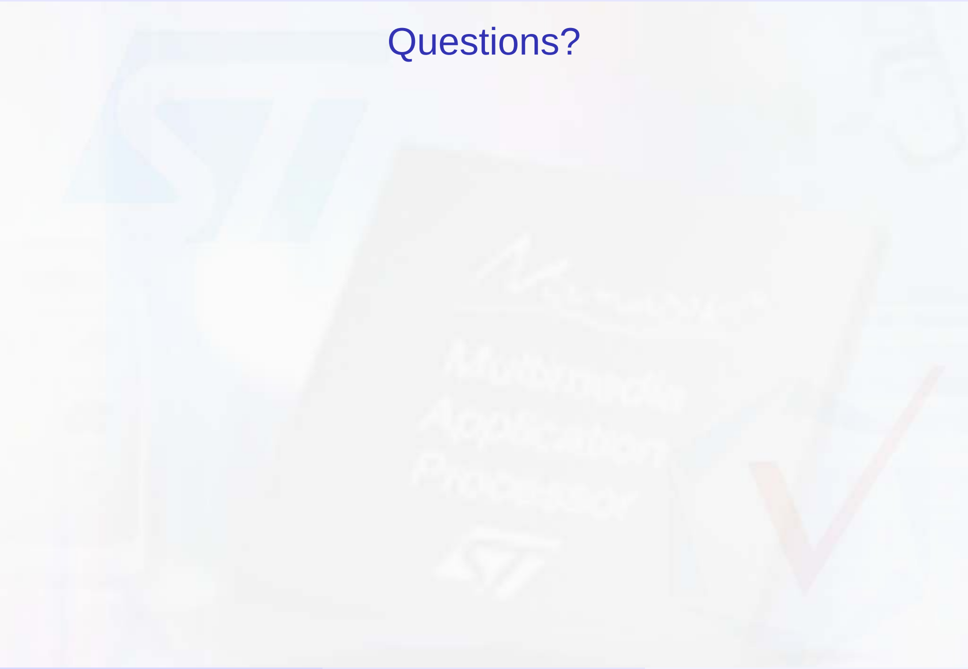
  - ▸ OpenTLM: A Minalogic project including STMicroelectronics, Verimag, Silicomp-AQL and others

Questions?



Backup slides

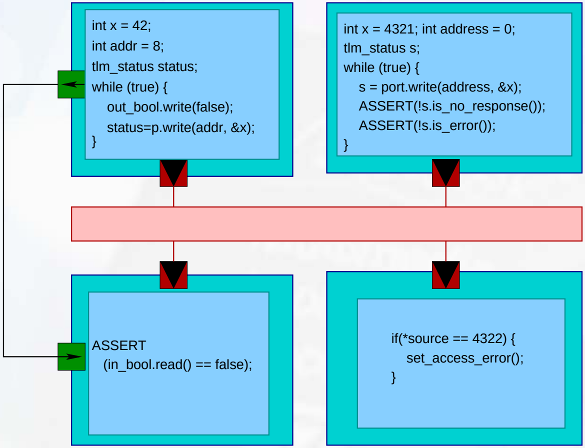
Users of PINAPA

- SPINAPA: SPIRIT back-end (Frédéric Saunier, STMicroelectronics/Silicomp)
- Theorem proving (Primrose Mbanefo)
- Platform Based Design Methodology (Humberto Rocha)
- Introspection in SystemC (Diogo Alves)
- Connection to PROMETHEUS (Yvan Roux, INRIA)
- 9 other subscribers on the mailing list.

PINAPA and dynamic objects

- No management of pointers/references to SystemC objects
- `port_array[42]` managed exactly as a normal port (because 42 is a constant)
- `port_array[x + y]`: PINAPA attaches a pointer to `port_array[0]` and the AST for “`x + y`”

Examples of Properties on a TLM



```
int x = 42;
int addr = 8;
tlm_status status;
while (true) {
    out_bool.write(false);
    status=p.write(addr, &x);
}
```

```
int x = 4321; int address = 0;
tlm_status s;
while (true) {
    s = port.write(address, &x);
    ASSERT(!s.is_no_response());
    ASSERT(!s.is_error());
}
```

```
ASSERT
  (in_bool.read() == false);
```

```
if(*source == 4322) {
    set_access_error();
}
```